REMARKS

Claims 1-23 are currently pending in the application. Claims 1, 6, 7, and 14 have been amended based on the description at page 13, lines 3-12 of the present specification.

On page 5 of the Office Action, claims 1, 2, 4-7, and 14 were rejected as being unpatentable over U.S. Patent No. 5,721,546 (Tsutsumishita) in view of U.S. Patent No. 5,400,148 (Kashida).

Applicants respectfully submit that neither Tsutsumishita nor Kashida, alone or in combination, discloses delaying an analog signal corresponding to a latency caused by the generation of a control signal to generate a delayed analog signal in an analog signal transmission path that is different from the analog signal process path (claim 1), delaying an analog signal corresponding to a latency caused by a generation of a control signal in synchronism with a clock signal to generate a delayed analog signal via the analog signal transmission path that is different from the analog signal process path (claim 6), a delay circuit, located in the analog signal transmission path that is different from the analog signal process path, for receiving the analog signal, and delaying an analog signal corresponding to a latency caused by the ADC and the digital arithmetic circuit to generate a delayed analog signal (claim 7), and a delay circuit, located in the analog signal transmission path that is different from the analog signal process path, for receiving the analog signal, and delaying the analog signal corresponding to a latency caused by the first control loop to generate a delayed analog signal (claim 14).

Rather, Tsutsumishita discloses A/D converters 8A, 8B and an arithmetic circuit 9 for converting digital data generated by the A/D converters 8A, 8B into position data (see column 1, lines 37-42 of Tsutsumishita).

Kashida discloses a synchronizing signal separation circuit 68 that separates horizontal anal vertical synchronizing signals from either the luminance signal input to the input terminal 10 or the external synchronizing signal input to the input terminal 64 and supplies the separated synchronizing signals to the timing control circuit 86 (see column 5, lines 8-23) . However, the circuit 68 of Kashida does not supply an analog signal (luminance signal) to the circuit 86 using an analog signal transmission path and does not delay the analog signal itself.

Further, Kashida discloses the timing control circuit 86 supplies to the color-differential signal sequential circuit 24 a timing signal whose passage has been delayed by a time corresponding to the time delay generated by the A/D converters 18 and 20 (see column 5, lines 15-18) .

However, Kashida does not delay an analog signal using an analog signal transmission path. Kashida only provides a timing signal generated by taking into account the signal delay of A/D converters 18 and 20. Moreover, the timing control circuit 86 of Kashida supplies the timing control circuit 88 for the frame memory 22, a synchronizing signal produced by delaying the passage of the synchronizing signal supplied from the synchronizing signal separation circuit 68 by a time. The time corresponds to the time delay generated by the color-differential signal sequential circuit 24 (see column 5, lines 19-25). However, Kashida does not delay an analog signal using an analog signal transmission path. Kashida uses the luminance signal Y and the color differential signals Pb and Pr as analog signals. However, Kashida does not delay any of the signals Y, Pb and Pr using an analog signal transmission path.

Accordingly, it is not possible to control an analog signal in synchronism with a digital control signal regardless of the process delay caused by analog-digital converting and arithmetic processing. By delaying an analog signal, the present invention can control a current analog signal as well as a future analog signal because an analog signal can be delayed independent of a digital signal. Consequently, the present invention is not obvious over Tsutsumishita in view of Kashida.

Claim 8 was rejected as being unpatentable over Tsutsumishita in view of Oishi et al.

Since claim 8 depends from claim 7 and neither Tsutsumishita nor Oishi discloses or suggests the above feature of the present invention of claim 7, Applicants respectfully submit that the present invention, as defined by claim 8 is not obvious over Tsutsumishita in view of Oishi.

Claims 12 and 13 were rejected as being unpatentable over Tsutsumishita in view of Gurvich et al. (U.S. Patent No. 6,897,724 hereinafter "Gurvich").

Since claims 12 and 13 each depend from claim 7 and neither Tsutsumishita nor Gurvich discloses or suggests the above-identified feature of the present invention, as defined by claim 7, Applicants respectfully submit that the present invention is not obvious over Tsutsumishita in view of Gurvich.

Applicants respectfully submit that all claims are patentable over the various cited combination of references for the reasons presented above.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: 23 April 07

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